REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Made corrections in table I. Editorial changes throuhout.	91-05-03	W. Heckman
B	Change to V_{CC} in paragraph 1.4 and table I.	99-05-13	K. A. Cottongim
C	Added new source of supply, (Satcon) with cage code 27851. Made corrections to table I for the input high current and gain error tests. Updated drawing to reflect the latest requirements of MIL-PRF-38534. -sld	04-01-20	Raymond Monnin

THE ORIGINAL FIRST PAGE OF THIS DRAWING HAS BEEN REPLACED

REV																				
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REV STATUS	REV	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

PMIC N/A	PREPARED BY Steve Duncan	**DEFENSE SUPPLY CENTER COLUMBUS** **COLUMBUS, OHIO 43216** **http://www.dscc.dla.mil**
STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A	CHECKED BY Robert M. Heber APPROVED BY William K. Heckman DRAWING APPROVAL DATE 90-07-23 REVISION LEVEL **C**	**MICROCIRCUIT, HYBRID, LINEAR, 8-BIT, FLASH, ANALOG TO DIGITAL CONVERTER** SIZE A | CAGE CODE **67268** | **5962-88776** SHEET 1 OF 14

DSCC FORM 2233
APR 97

5962-E112-04

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing describes device requirements for class H hybrid microcircuits in accordance with MIL-PRF-38534.

1.2 PIN. The PIN shall be as shown in the following example:

5962-88776	01	X	X
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	HS1068, SP-2069	A/D converter, 8-bit flash

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	24	Dual-in-line

1.2.3 Lead finish. The lead finish shall be as specified in MIL-PRF-38534.

1.3 Absolute maximum ratings. 1/

Positive supply voltage range (V_{CC})	+0.5 V dc to +7.0 V dc
Negative supply voltage (V_{EE})	-7.0 V dc
Digital input voltage	+5.5 V dc
Analog input voltage	±5.5 V dc
Reference voltage	2.2 V dc
Applied output voltage	5.5 V dc
Power dissipation (T_C = +125°C)	3.0 W
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+300°C
Junction temperature (T_J)	+150°C
Thermal resistance, junction-to-case (Θ_{JC})	40°C/W

1.4 Recommended operating conditions.

Positive supply voltage range (V_{CC})	+4.75 V dc to +5.25 V dc
Negative supply voltage range (V_{EE})	-4.9 V dc to -5.5 V dc
Analog ground voltage range (V_{AGND})	-0.1 V dc to +0.1 V dc
Digital input high voltage (V_{IH})	2.0 V dc minimum
Digital input low voltage (V_{IL})	0.8 V dc maximum
Applied output voltage (V_O)	V_{CC}
R_{BOT} adjustment range (R_{ADJ})	±0.2 V 2/
Convert pulse width low (t_{PWL})	18 ns minimum
Convert pulse width high (t_{PWH})	22 ns minimum
Maximum clock frequency (f_{CLK})	20 MHz minimum
Case operating temperature range (T_C)	-55°C to +125°C

1/ Stresses above the absolute maximum ratings may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ Operation is possible down to R_{BOT} = -1.1 V with reduced dynamic performance.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38534 - Hybrid Microcircuits, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbook are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.).

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item performance requirements for device class H shall be in accordance with MIL-PRF-38534. Compliance with MIL-PRF-38534 may include the performance of all tests herein or as designated in the device manufacturer's Quality Management (QM) plan or as designated for the applicable device class. Therefore, the tests and inspections herein may not be performed for the applicable device class (see MIL-PRF-38534). Futhermore, the manufacturers may take exceptions or use alternate methods to the tests and inspections herein and not perform them. However, the performance requirements as defined in MIL-PRF-38534 shall be met for the applicable device class.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38534 and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Block diagram(s). The block diagram(s) shall be as specified on figure 3.

3.2.4 Output coding table(s). The output coding table(s) shall be as specified on figure 4.

3.2.5 Timing diagram(s). The timing diagram(s) shall be as specified on figure 5.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full specified operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking of device(s). Marking of device(s) shall be in accordance with MIL-PRF-38534. The device shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's vendor similar PIN may also be marked.

3.6 Data. In addition to the general performance requirements of MIL-PRF-38534, the manufacturer of the device described herein shall maintain the electrical test data (variables format) from the initial quality conformance inspection group A lot sample, for each device type listed herein. Also, the data should include a summary of all parameters manually tested, and for those which, if any, are guaranteed. This data shall be maintained under document revision level control by the manufacturer and be made available to the preparing activity (DSCC-VA) upon request.

3.7 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to supply to this drawing. The certificate of compliance (original copy) submitted to DSCC-VA shall affirm that the manufacturer's product meets the performance requirements of MIL-PRF-38534 and herein.

3.8 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38534 shall be provided with each lot of microcircuits delivered to this drawing.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38534 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. Screening shall be in accordance with MIL-PRF-38534. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to either DSCC-VA or the acquiring activity upon request. Also, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) T_A as specified in accordance with table I of method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $+4.75\ V\ dc \le V_{CC} \le +5.25\ V\ dc$ $-4.9\ V\ dc \le V_{EE} \le -5.5\ V\ dc$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Resolution	RES		1,2,3	01		8.0	Bits
Integral linearity error	E_{LI}	DC, best straight line	1	01	-0.5	+0.5	LSB
			2,3		-1.0	+1.0	
Differential linearity error	E_{DI}	DC	1,2,3	01	-0.75	+0.75	LSB
Code size	CS		4,5,6	01	25	175	%
Full power bandwidth	FPBW	No spurious codes	4	01	7.0		MHz
			5,6		5.0		
Range amplifier 1/ bandwidth	RABW		4,5,6	01	100		kHz
Range amplifier settling time	t_S	One volt step at R_{BOT}	9,10,11	01		50	µs
Maximum conversion rate	f_S	V_{CC} = +4.75 V, V_{EE} = -4.9 V	9,10,11	01	20		MHz
Sampling time offset 1/	t_{STO}	V_{CC} = +4.75 V, V_{EE} = -4.9 V, See figure 5	9,10,11	01		10	ns
Digital output delay 1/	t_D	V_{CC} = +4.75 V, See figure 5	9,10,11	01	15	28	ns
CONV pulse width, low 1/	t_{PWL}	V_{CC} = +4.75 V	9,10,11	01	18		ns
CONV pulse width, high 1/	t_{PWH}	V_{CC} = +4.75 V	9,10,11	01	22		ns
Input low current	I_{IL}	NMINV, NLINV	1,2,3	01		-2.8	mA
		$\overline{OE}$				-0.4	
		CONV				-0.8	
Input high current	I_{IH}	NMINV, NLINV	1,2,3	01	-1340	50	µA
		$\overline{OE}$				20	
		CONV				70	
Input low voltage 1/	V_{IL}		1,2,3	01		0.8	V
Input high voltage 1/	V_{IH}		1,2,3	01	2.0		V
Analog input resistance 1/	R_{IN}		4,5,6	01		1.0	kΩ
Output leakage current, logic low	I_{LOL}		1,2,3	01		-20	µA

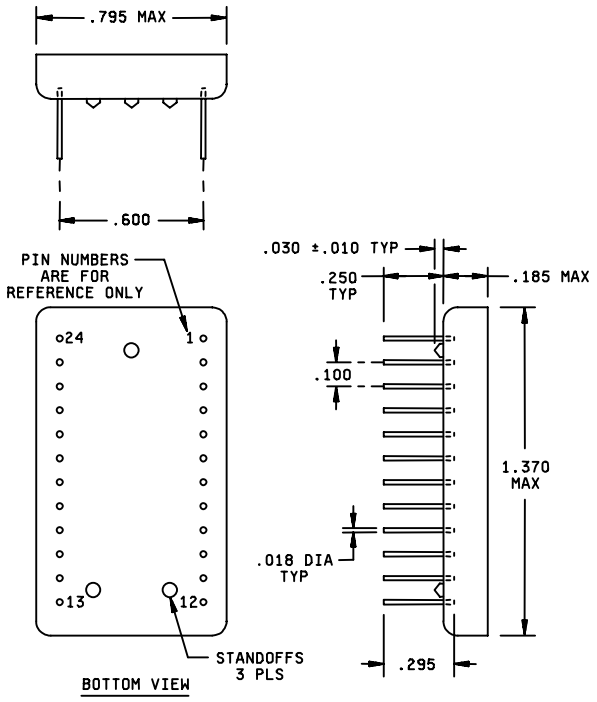
See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $+4.75\ V\ dc \le V_{CC} \le +5.25\ V\ dc$ $-4.9\ V\ dc \le V_{EE} \le -5.5\ V\ dc$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Output leakage current, logic high	I_{LOH}		1,2,3	01		20	µA
Output voltage low	V_{OL}	I_{OL} = 12 mA	1,2,3	01		0.4	V
Output voltage high	V_{OH}	I_{OH} = -1.0 mA	1,2,3	01	2.4		V
Output short circuit current 1/	I_{OS}	V_{CC} = +5.25 V, Output high	1,2,3	01	-30	-130	mA
Reference voltage	V_{REF}	V_{REF} output	1,2,3	01	1.18	1.26	V
Reference regulation	ΔV_{REF}	1200 Ω, V_{REF} to GND, 0 to 1 mA load	1,2,3	01	-6.3	6.3	mV
Digital supply current, static	I_{CC}	V_{CC} = +5.25 V, 1.1 MHz FS input, one LSTTL load, dc input, output codes = low	1	01		150	mA
			2,3			200	
Analog supply current, static	I_{EE}	V_{EE} = -5.5 V, 1.1 MHz FS input, one LSTTL load, dc input, output codes = low	1	01		290	mA
			2,3			340	
Input amplifier frequency response		Full scale, 20 MHz input signal	4	01	-3.4	-1.0	dB
			5,6		-4.0	-1.0	
Gain error	G_E	Zero to full scale	1,2,3	01	-1.0	+1.0	%
Bipolar offset error	V_{OS1}	Midscale input	1	01	-5.0	+5.0	LSB
			2,3		-6.0	+6.0	
Unipolar offset error	V_{OS2}	Lowscale input	1	01	-5.0	+5.0	LSB
			2,3		-6.0	+6.0	
Signal-to-noise ratio rms signal/rms noise and distortion	SNR	1.1 MHz input	4	01	45		dB
			5,6		43		
		9.7 MHz input	4		32		
		8.1 MHz input	5,6		32		

1/ Parameter shall be tested as part of device characterization and after design and process changes. Parameter shall be guaranteed to the limits specified in table I for all lots not specifically tested.

Case outline X.



Inches	mm
.010	0.25
.018	0.46
.030	0.76
.100	2.54
.185	4.70
.250	6.35
.295	7.49
.600	15.24
.795	20.20
1.370	34.80

NOTES:
1. Dimensions are in inches.
2. Metric equivalents are given for general information only.
3. Unless otherwise specified, tolerance is ±.005 (0.13 mm).
4. Standoffs are optional at discretion of the manufacturer.

FIGURE 1. Case outline(s).

Device type		01
Case outline		X
Terminal		Function
number	symbol	
1	REF	Refrerence output
2	RANGE	Gain adjust input
3	R_{BOT}	Test point
4	V_{EE}	Negative supply voltage
5	NMINV	Not most sigificant bit invert
6	V_{CC}	Positive supply voltage
7	$\overline{FS}$	Full scale low, overflow detector
8	$\overline{OE}$	Output enable
9	D1 (MSB)	Data bit 1
10	D2	Data bit 2
11	D3	Data bit 3
12	D4	Data bit 4
13	D5	Data bit 5
14	D6	Data bit 6
15	D7	Data bit 7
16	D8 (LSB)	Data bit 8
17	ZS	Zero scale, underflow detector
18	D_{GND}	Digital ground
19	CONV	Convert
20	NLINV	Not least significant bits invert
21	A_{OUT}	Test point (amplifier output)
22	A_{GND}	Analog ground
23	A_{IN}	Analog signal input
24	OFFSET	Offset adjust

FIGURE 2. Terminal connections.

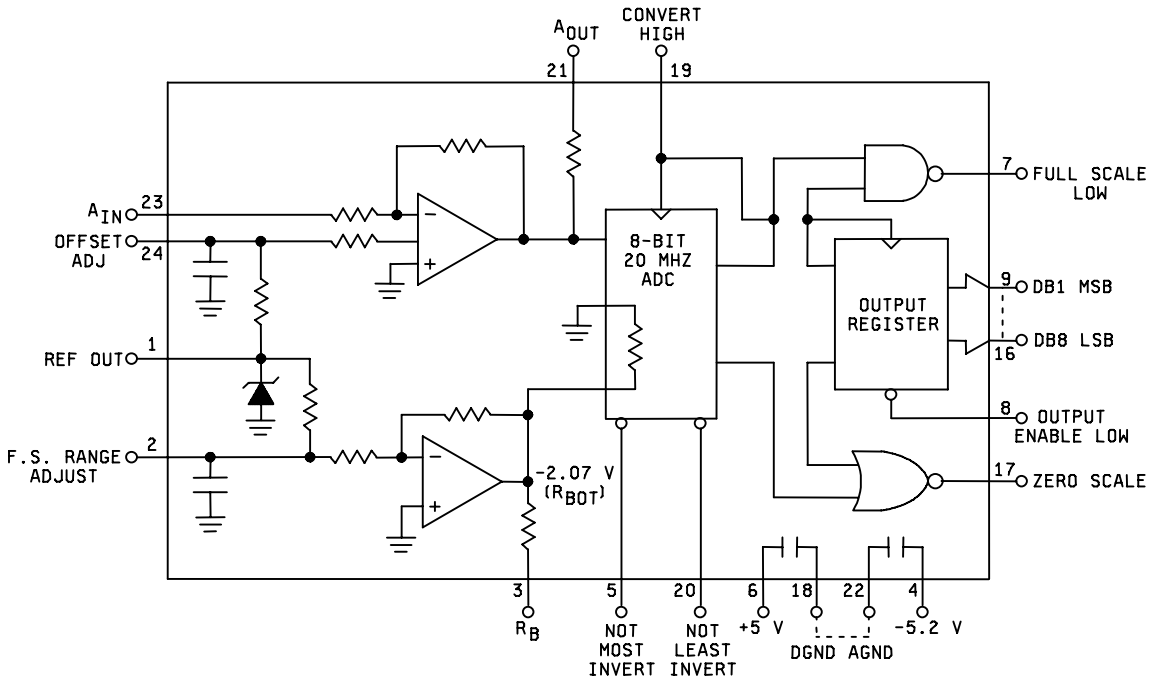
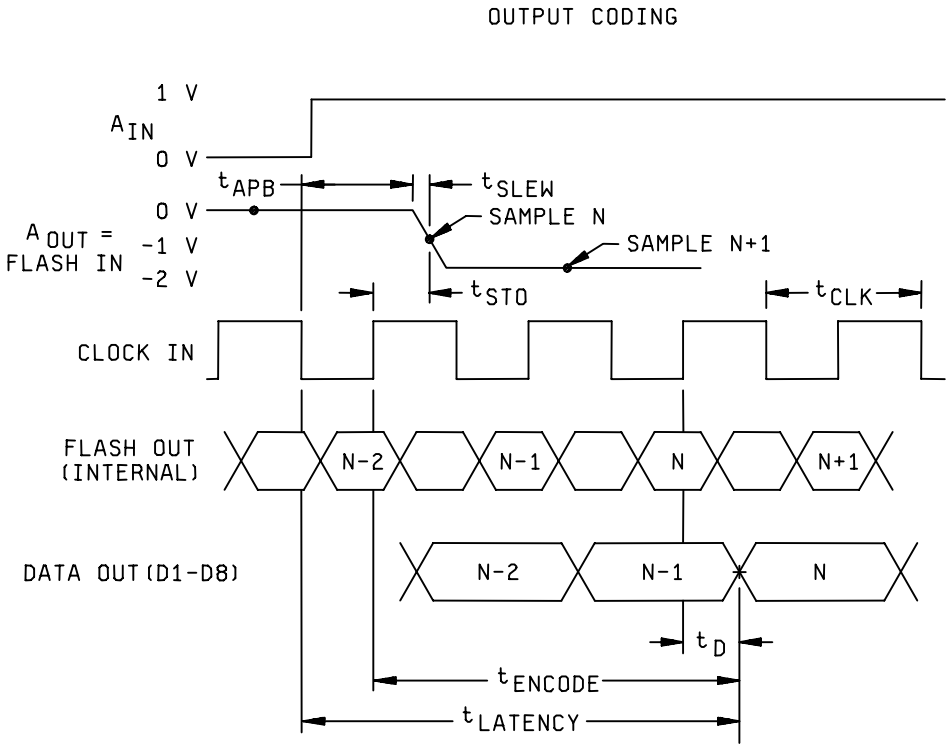


FIGURE 3. Block diagram.

Input voltage code center in unipolar mode	Binary		Two's complement	
	True	Inverted	True	Inverted
	NMINV-1 NLINV-1	0 0	0 1	1 0
0.0000	00000000	11111111	10000000	01111111
+0.0039	00000001	11111110	10000001	01111110
*	*	*	*	*
*	*	*	*	*
*	*	*	*	*
+0.4960	01111111	10000000	11111111	00000000
+0.5000	10000000	01111111	00000000	11111111
*	*	*	*	*
*	*	*	*	*
*	*	*	*	*
+0.9920	11111110	00000001	01111110	10000001
+0.9960	11111111	00000000	01111111	10000000

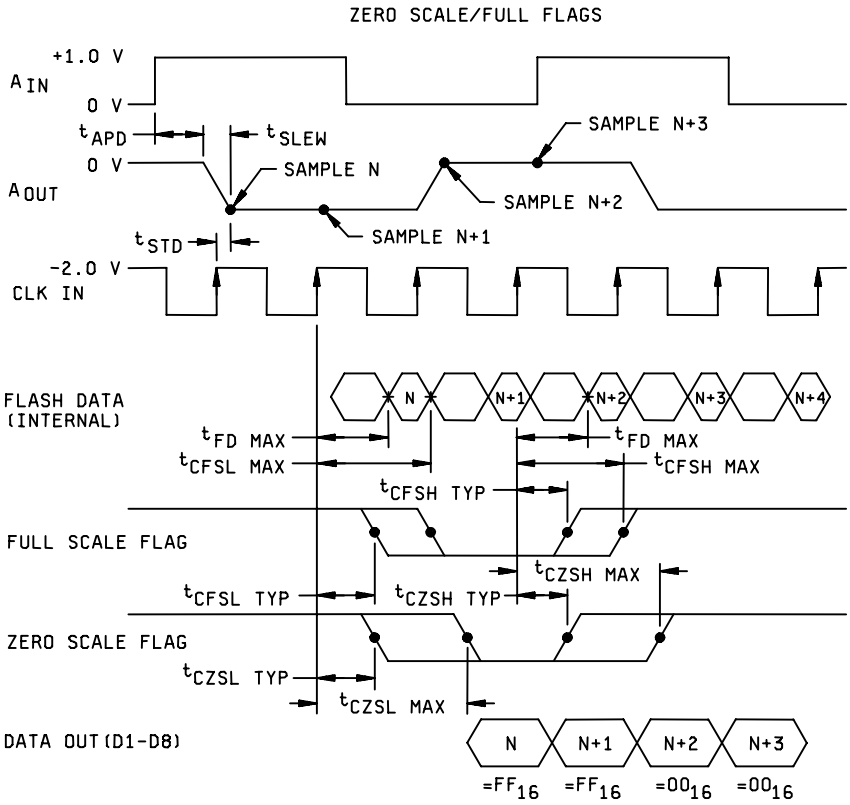
NOTE: Input voltages are at code centers and buffer amplifier offset voltage is nulled.

FIGURE 4. Output coding table.



NOTES:
1. Amplifier propagation delay (t_{APD}) = 30 ns typically.
2. Amplifier slewing time (t_{SLEW}) = 5 ns typically.
3. One convert clock cycle (t_{CLK}) = 50 ns for (20 MHz sampling).
4. ($t_{LATENCY}$) = 2(t_{CLK}) + t_D - t_{STO} + t_{APD} + t_{SLEW} = 140 ns.

FIGURE 5. Timing diagram(s).



NOTES:

1. t_{FD}MAX = Internal flash data delay = 35 ns maximum.
2. t_{CFSL} = Clock to $\overline{FS}$ flag asserted (low) = 25 ns typically.
3. t_{CZSH} = Clock to ZS flag asserted (high) = 29 ns typically.
4. t_{OVFSL} = Overvoltage into $\overline{FS}$ (low) = 100 ns typically.
5. t_{UVZSH} = Undervoltage to ZS (HIGH) = 105 ns typically.

FIGURE 5. Timing diagram(s) - Continued.

TABLE II. Electrical test requirements.

MIL-PRF-38534 test requirements	Subgroups (in accordance with MIL-PRF-38534, group A test table)
Interim electrical parameters	1
Final electrical parameters	1*,2,3,4,5,6,7
Group A test requirements	1,2,3,4,5,6,7,8,9,10,11
Group C end-point electrical parameters	1,2,3,4,9
End-point electrical parameters for Radiation Hardness Assurance (RHA) devices	Not applicable

* PDA applies to subgroup 1.

4.3 Conformance and periodic inspections. Conformance inspection (CI) and periodic inspection (PI) shall be in accordance with MIL-PRF-38534 and as specified herein.

4.3.1 Group A inspection (CI). Group A inspection shall be in accordance with MIL-PRF-38534 and as follows:

a. Tests shall be as specified in table II herein.

b. Subgroups 7 and 8 tests shall be sufficient to verify the output coding table.

c. Subgroups 9, 10, and 11 shall be tested as part of device initial characterization and after design and process changes. Parameters shall be guaranteed to the limits specified in table I for all lots not specifically tested.

4.3.2 Group B inspection (PI). Group B inspection shall be in accordance with MIL-PRF-38534.

4.3.3 Group C inspection (PI). Group C inspection shall be in accordance with MIL-PRF-38534 and as follows:

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to either DSCC-VA or the acquiring activity upon request. Also, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

(2) T_A as specified in accordance with table I of method 1005 of MIL-STD-883.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.3.4 Group D inspection (PI). Group D inspection shall be in accordance with MIL-PRF-38534.

4.3.5 Radiation Hardness Assurance (RHA) inspection. RHA inspection is not currently applicable to this drawing.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38534.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated as specified in MIL-PRF-38534.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-1081.

6.6 Sources of supply. Sources of supply are listed in MIL-HDBK-103 and QML-38534. The vendors listed in MIL-HDBK-103 and QML-38534 have submitted a certificate of compliance (see 3.7 herein) to DSCC-VA and have agreed to this drawing.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 04-01-20

Approved sources of supply for SMD 5962-88776 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38534 during the next revisions. MIL-HDBK-103 and QML-38534 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revisions of MIL-HDBK-103 and QML-38534.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8877601XA	3/	HS1068B
5962-8877601XA	27851	SP-2069
5962-8877601XC	3/	HS1068B
5962-8877601XC	27851	SP-2069

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the Vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ This device is no longer available.

Vendor CAGE number	Vendor name and address
27851	SatCon Electronics 165 Cedar Hill Street Marlborough, MA 01752